Inkjet-Deposited Interconnections for Electronic Packaging

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Abstract

Inkjet technology provides an interesting approach for electronic manufacturing. Small volumes of functional material e.g., conductive ink are dispensed on top of the substrate. Electrical circuits are formed by suitable printing sequence and sintering processes. In this paper, we present a concept of inkjet deposited System-in-Package (SiP). The package contains bare ICs and discrete passive components that are encapsulated with resin mold. Encapsulation material works as a substrate for interconnections, which are directly deposited on top of the mold. All connections between the components and connections to the I/O pins are formed by inkjetting silver nano-particle and dielectric inks. Silver nano-particles are sintered in an oven at 220°C and resistivity values lower than 5 μΩcm are reported. Pre-curing of a substrate in a higher temperature than the sintering temperature of silver nano-particles, decreases the resistivity of the lines. As a conclusion, the sintering profile needs to be considered carefully in order to achieve resistance requirements set by the design. This paper focuses on interconnections and system integration design aspects.

Introduction

Today's electronic production is a complex logistical operation that requires the management of several phases for example manufacturing of a main board, mechanics, and components, assembly, and packaging. This kind of production does not allow high flexibility and cannot respond to fast product customization. As a solution, inkjet technology provides an interesting option for producing electrical circuits, and is therefore received a lot of interest in electronic packaging [1, 2, 3]. In inkjet technology, small droplets of functional materials are deposited on top of the substrate or directly onto the mechanics of the device. Electrical circuits are formed with a proper jetting sequence and sintering profiles enabling new integration approaches and customization of products. The advantage of the inkjet technology in comparison to current mainstream electronic manufacturing technologies is that it is flexible and a fully-additive manufacturing process. Digital printing is flexible in terms of products and volumes. Every printed image can be different, which indicates that theoretically every product can be customized based on the customer needs. Even different products can be manufactured in the same production line. Furthermore, inkjet is also suitable for mass production. Printing of electronics differs a lot the from printing of graphics, but developments in graphic inkjet machines and the infrastructure will definitely help to create new business models, infrastructure, and value networks.

In this paper, we discuss inkjet deposited interconnections in electrical packages. We evaluate the capability of inkjet technology through a System-in-Package (SiP) application. In SiP several components, including actives and passives, are integrated inside a package and all interconnections between the components and I/O pins are printed with inkjet.

Concept of Inkjetted SiP

This paper focuses on inkjetted interconnections in electronic packaging. The proposed SiP structure contains encapsulated components, and all electrical connections between the components and I/O pins are inkjetted using silver nano-ink for conductors and heat curable isolating material for the dielectric layers.

The manufacturing process of a module is shown in Figure 1. At the beginning, components are assembled on an adhesive carrier. High accuracy is essential due to small pitch values in ICs. Alignment is more important than in the conventional SMD process, because of the lack of self-alignment capability. Contact areas of the components must be placed towards the carrier. After the component assembly, the carrier is placed in the molding cast and the epoxy resin is poured inside the case. Basically, there are two options for molding. Modules can be encapsulated separately or several modules can be placed inside the same frames and modules are separated from the sheet by cutting.

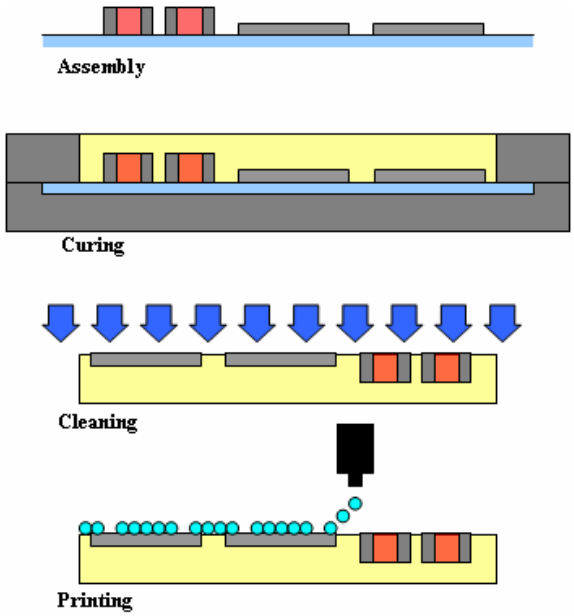

Figure 1. *Process steps of inkjet printed System-in-Package manufacturing.*

Narrow gaps between the components need to be full-filled, which sets strict requirements for the viscosity of the molding material. The denser the layout is, the lower the viscosity must be. Also, the surface of the adhesive carrier needs to be suitable for mold material. Furthermore, thermo-mechanical properties must be considered during the material selection. In general, material

with low modules and coefficient of thermal expansion (CTE) is needed in order to minimize thermo-mechanical stresses and warpage in the package. The CTE value can be decreased with e.g. silica particles in order to match it better with the components. However, particle size must be small enough to allow proper filling of the gaps. Furthermore, the warpage of the package can be controlled by changing the component placements or with an additional foil attached on the other side of the package [4].

Next, the resin is cured in an elevated temperature. During the encapsulation process modules need to be exposed to the higher temperatures than the processing temperatures of other materials in order to achieve a thermally and mechanically stable structure. In the final phase, the carrier is removed and the surface is cleaned of residuals with oxygen plasma. Even small contaminations and residues can affect the reliability, quality, and yield of the structure. Since, plasma cleaning improves the wettability of the surface, it is highly recommended when smooth layers are needed.

After the molding process the module is ready for the printing. Components are placed in the mold contact side uppermost and the encapsulation material works as a substrate for interconnections. The forming of the electrical circuit with inkjet technology is based on low temperature sintering of nano-sized metal particles and dielectric fluids. The melting point of the nano-sized particles is significantly lower than the melting point of the bulk material due to increased number of surface atoms compared to inner atoms, and therefore interactions between the atoms diminish [5]. The silver NanoPaste® used in this study requires sintering temperature of 220-230 °C for a period of one hour [6], which will introduce quite a tough thermal stress for the components. Thus, material selection must be considered. In order to reduce heat stresses, more advantage sintering methods, such as laser or microwave sintering can be used [7, 8, 9]. Figure 2 shows an example of encapsulated components with first level interconnections. This module has a size of 17 mm x 17 mm x 1.0 mm, containing four bare ICs and over 50 discrete passive components.

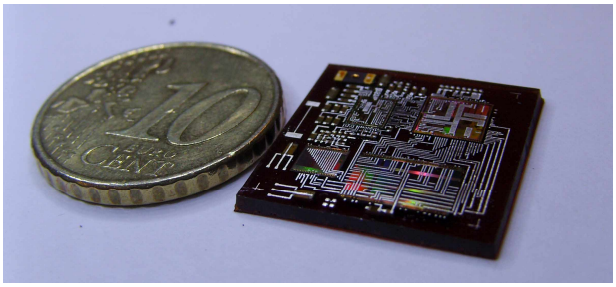

Figure 2. *Encapsulated components and first level interconnections inkjetted. Module has a size of 17 mm x 17 mm x 1 mm.*

Printing Process

Typically, mainstream electronics uses subtractive manufacturing methods, such as etching, to produce wiring. Creating interconnections with inkjet technology is, however, an additive process, which has some advantages compared to subtractive methods. First of all, the number of process steps is decreased and manufacturing process is simplified. The etching process contains several stages: mask creation, resist placement, exposing, cleaning, etc. These steps are replaced with material jetting and sintering. Furthermore, additive manufacturing process provides a more environmental friendly approach to manufacture electronics due to decreased amount of waste, because material is placed only where it has a function. The process is controlled with computer by printing the files. This enables an extremely flexible manufacturing environment.

In the beginning before printing can be started, interactions between substrate and ink must be examined. Good process conditions can be found by varying the temperature, surface material concentration, and jetting algorithm. First, the surfaces of the modules need proper treatment to ensure good wetting properties and adhesion between the substrate and inkjetted material. First of all, the surface must be cleaned of residuals and other impurities. This is done with oxygen plasma or UV-ozone. After the cleaning, the surface energy of the substrate is very high causing complete wetting and spreading of the ink. The contact angle between the drop and substrate can be increased by adding surfactants to the ink or by adding surface treatment material on top of the substrate. The latter approached is preferred, because then the ink can be used for several substrates, otherwise ink must be customized for each substrate. However, for high volume manufacturing ink modification might be a more cost effective solution. We added fluorine based chemical 3M's EGC-1720 in order to control the contact angle. Larger contact angle decreases the diameter of the drop. If the contact angle between the substrate and the drop is small, the drop will spread and high resolution pictures cannot be produced. Decrease in the relative surface energy creates a larger contact angle and makes enables high resolution pictures. On the other hand, there is a trade off between the resolution and adhesion, because a high contact angle usually indicates lower adhesion [10].

From the miniatyrization point of view, narrow lines are preferred. In inkjet technology, the highest resolution that can be used depends on drop placement accuracy, drop volume, and interactions between the substrate and the ink. Current ICs have a pitch size around 60 µm and pad size around 40 µm or even smaller. Drop placement accuracy must be much better than this. As a thumb rule, drop placement accuracy must be one decade of the line width. Minimum line width depends on the drop volume. Current printheads have a drop volume between 1 pl to 100 pl. The smaller the drop volume is, the smaller the minimum line width is. For example 10 pl printhead creates a drop that has a diameter of 35 µm to 45 µm depending on interactions between the substrate and the ink. A one picolitre printhead produce drops with diameter around 20 µm. Figure 3 illustrates the difference between 1 pl and 10 pl drops on polyimide substrate with different surface treatment condition and Figure 4 presents the drop diameter as a function of the surface treatment material concentration.. These figures show how the drop diameter is decreased when the surface treatment material concentration is increased. It can be seen that even small concentration values influences the drop diameter. However, after increasing the concentration the trend of the curve becomes smoother. These drop diameters are small enough for IC connections. Additionally, very small drop volumes in the order of femtolitres are reported in article [11].

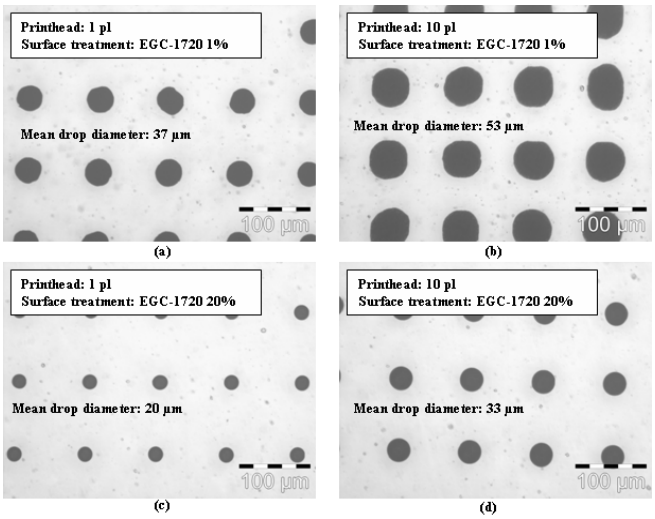

Figure 3. *Inkjetted drops on top of the polyimide substrate a) 1 pl drop with 1% surface treatment, b) 10 pl drop with 1% surface treatment, c) 1 pl drop with 20% surface treatment, d) 10 pl drop with 20% surface treatment.*

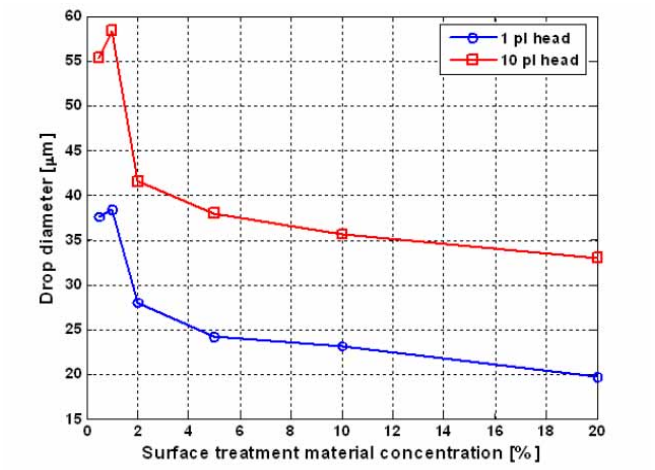

Figure 4. *The effect of the surface treatment material concentration. Curve with circles presents the drop diameter values from 1 pl printhead and curve with squares presents drop diameter from 10 pl printhead.*

One of the key things to printing high resolution patterns is the use of a suitable printing algorithm. If a high resolution pattern is printed without sequential manner, ink will overflow causing short circuits or drops join together forming bigger drops that cause bulking of lines and open circuits. Which one will occur depends on the interactions between the substrate and the ink. Figure 5 presents this phenomenon. If the drops are printed simultaneously, drops gather together to form bigger drops. This will cause bulking of lines. If the picture is divided into four parts that are printed one after another, bulking of lines is avoided.

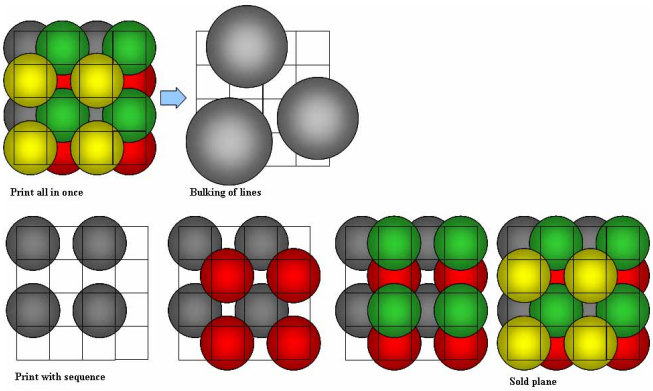

Figure 5*. If all data is printed simultaneously, lines are bulking. Solid plane is achieved with a proper jetting algorithm.*

In most of cases the first interconnection layer is the most challenging one to print, because it contains the interconnections to ICs and other components. Finding of right process conditions is quite challenging due to multiple material interfaces. The conditions need to fit with the mold, ICs, and passives. In addition, the first layer usually has the highest design rule requirements due to the number of I/O pins on ICs. After the correct parameters are found, layers can be created. One layer contains three phases.

In the first phase, vias are printed on top of the passive components, ICs, or contact pads. The height of the vias can be increased by printing the same file several times. Nano-particles are sintered in the oven after the printing. In the next phase, dielectric material is printed on top of the module by leaving via holes open. The other possibility would be that the dielectric is printed only on the places of crossovers. However, it would create topography on top of the module, which might cause some issues later depending on how the system is attached to other devices. The selected approach creates a smooth layer suitable for additional printing. In the final phase, the conductive layer is printed. Figure 6 shows the connection of an IC. A multilayer structure is created by repeating the phases. Figure 7 shows via connections through the ground plane.

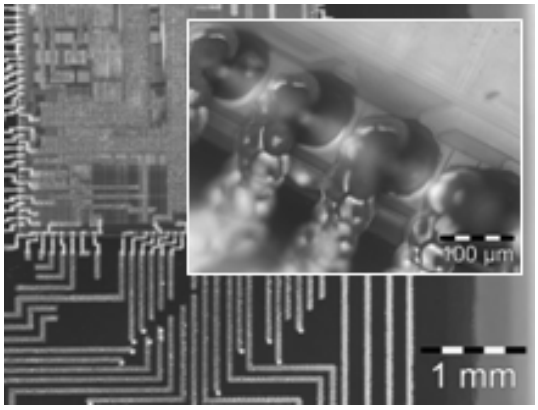

Figure 6. *IC connection created with inkjet.*

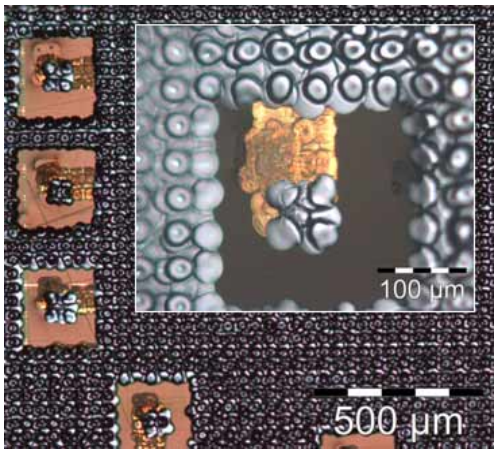

Figure 7. *Via connections through the ground plane.*

Electrical Design

From an electrical point of view, the resistance of a conductor is the most important parameter. The resistance increases the losses of the line causing heat dissipation and voltage drops along the trace. The resistance depends on the resistivity of the material, length of the line, and the cross-sectional area of the line. Resistance can be decreased by decreasing the resistivity or the length and by increasing the width or thickness of lines. The resistivity of printed conductors is usually higher than the resistivity of bulk materials. It is increased due to imperfections in material e.g., surfactants, surface roughness, and the electrical contact between particles. Resistivity of the silver nano-particles depends on the sintering temperature and time [6]. The sintering time can be decreased by increasing the sintering temperature.

For high performance systems, voltage drops along the signal line or in power/ground planes might cause unwanted behavior of the system. Therefore, systems should be designed in such a manner that voltage drops are not so critical. In many applications a voltage drop of few hundred millivolts is usually acceptable, but higher voltage drops are not. Therefore, it is very important to optimize the process in order to decrease the resistance. Normally, resistance is decreased by increasing the line width or thickness. However, in miniaturized design, it is usually quite hard to increase the line width and an increase in thickness increases the risk of cracking, which is caused by the shrinkage of the printed traces during the sintering profile. Shrinking of the lines introduces stresses, which can cause delamination between the lines and dielectric layers. The risk of cracking increases with thicker layers. Stresses can be reduced with proper design. For example using of small holes in ground plane or grid ground decreases the stresses, but on the other hand increases the impedance and introduces higher voltage drops. Suitability of grid ground depends on the application.

In order to create design rules for inkjetted SiP we characterized the resistivity of printed traces on different substrates. The test pattern is shown in Figure 8. It contains several lines that have a length of 10 mm, width of the line is 100 µm, and the thickness 1.76 µm. The ends of lines contain a square contact pads that have an edge length of 1.0 mm.

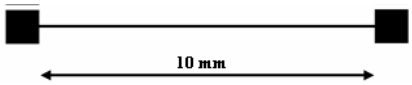

Figure 8. *Test pattern consists of several 10 mm lines, which have a line width of 100 µm.*

We studied the effect of substrate material and pre-curing profile with the conductivity of the traces. Seven test sets were investigated and each set contains several lines. All the samples were sintered in an oven at 220 °C at one hour. Test parameters and resistance values are listed in Table I. The Set A test pattern is printed on top of polyimide film. In Sets B, C, and E, test patterns were the printed on top of the cured epoxy resin and in Sets E, F, and G on top of the cured epoxy that has a printed dielectric layer on top of the surface, as shown in Figure 9. Sets B and E were not pre-cured. Sets C and F were pre-cured in an oven at 220 °C at one hour, and sets D and G were pre-cured in oven at 220 °C at one hour and then an additional six minutes at 250 °C.

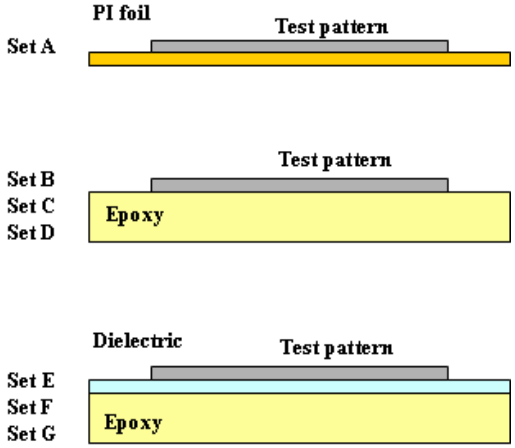

Figure 9. *Test patterns are printed on top of substrate in Set A. In Sets B, C, and D the substrate is the epoxy, and in the case of Sets E, F, and G the test structures are printed on top of the dielectric material.*

Table I. Sheet resistances and resistivities of the test sets.

Set	Substrate	Pre-cure	Sheet resistance [mΩ□]	Resistivity [µΩcm]
A	Polyimide	-	27.1	4.8
B	Epoxy	-	65.4	11.5
C	Epoxy	220˚C 1h	62.3	11.0
D	Epoxy	220˚C 1h + 250˚C 6min	39.1	6.9
E	Epoxy + Dielectric	-	172	30.3
F	Epoxy + Dielectric	220˚C 1h	60.0	10.55
G	Epoxy + Dielectric	220˚C 1h + 250˚C 6min	45.6	8.0

From Table I, it can be seen that the lowest resistivity was achieved with Set A and Set E has the poorest conductivity. Set A has a resistivity value of 4.8 μΩcm. In comparison to the bulk silver resistivity, which is 1.6 μΩcm, the printed trace has a three times larger resistivity than the bulk material. Furthermore, results indicate that pre-curing of samples decreases the resistivity, and pre-curing temperature should be higher than the sintering temperature of the conductive ink. Decreased resistivity is a result of smaller outgassing, which harms the sintering profile. Polyimide has a very small outgassing and also the Sets D and F have smaller outgassing in sintering temperature, because of the high pre-curing temperature.

Conclusions

In this paper we evaluated the capability of inkjet technology for electronic packaging and presented a concept of SiP, which is manufactured using inkjet technology. Parameters affecting to the high resolution printing and electronic miniaturization were discussed.

The diameter of a drop depends on the drop volume and the interactions between the surface and the ink. With a one picolitre printhead, diameters as small as 20 μm can be produced. This is small enough in order to connect most of the current ICs. We demonstrated high resolution printing by connecting an IC. Furthermore, it is very important to use a proper jetting algorithm. Otherwise, the design might suffer from over flooding or bulking of lines. It was proven that the pre-curing of the mold resin is essential and remarkable decrease in resistivity can achieved.

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